

# David C. Walter

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## Education

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- *Ph.D. Computer Science, University of Utah, Salt Lake City, Utah* August 2007  
**Advisor:** Dr. Chris Myers  
**Research:** Verification of analog and mixed-signal circuits using symbolic methods.  
**Related Courses:** CAD of Digital Circuits, Formal Methods in System Design, Synthesis and Verification of Asynchronous VLSI Systems, and Digital VLSI Design.
- *B.S. Computer Science, University of Utah, Salt Lake City, Utah* May 2001
- *B.S. Computer Engineering, University of Utah, Salt Lake City, Utah* May 2001

## Work Experience

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- *Research Assistant, University of Utah* January 2003–May 2007  
Developing hybrid Petri net model and model-checking tool based on BDDs for the analysis of mixed-signal/analog systems. Applying abstraction techniques to improve performance.
- *Instructor, University of Utah* Summer 2001 and Summer 2002  
Prepared and presented all course content for courses in introductory Java and C++.
- *Teaching Assistant, University of Utah* September 1997–December 2002 (noncontinuous)  
Lead classroom discussions, graded exams and homework, and answer student questions for introductory computer science classes and digital design class.
- *Student Consultant, Microsoft* August 2000–May 2001  
Worked with faculty to help integrate Microsoft technology into appropriate curriculum. Organized events and presented technical talks to promote student interest in Microsoft technology.
- *Software Design Engineer in Test (Intern), Microsoft* May 2000–August 2000  
Investigated and applied testing methodologies of existing projects in implementation of test plan for new project in Windows CE Tools Group.
- *Software Design Engineer in Test (Intern), Microsoft* May 1999–August 1999  
Designed and developed web applications using Active Server Pages and SQL Server technology for the Windows NT Build group.
- *Technical Writing Co-Op, Unisys* June 1997–September 1997  
Worked in the Product Information group to write, index, and edit technical documentation for Unisys products ranging from peripherals to mainframes.

## Selected Publications

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- D. Walter, S. Little, N. Seegmiller, C. Myers, and T. Yoneda, "Symbolic model checking of analog/mixed-signal circuits," to appear in *12th Asia and South Pacific Design Automation Conference (ASPAC)*, January, 2007, pp. 316–323.
- S. Little, N. Seegmiller, D. Walter, C. Myers, and T. Yoneda, "Verification of analog/mixed-signal circuits using labeled hybrid Petri nets," to appear in *International Conference on Computer-Aided Design (ICCAD)*, November, 2006, pp. 275–282.
- C. Myers, R. Harrison, D. Walter, N. Seegmiller, and S. Little, "The case for analog circuit verification," in *Electronic Notes in Theoretical Computer Science (ENTCS)*, June, 2006, 153(3): 53–63.
- H. Zheng, C. Myers, D. Walter, S. Little, and T. Yoneda, "Verification of timed circuits with failure directed abstractions," in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, March, 2006, 25(3): 403–412.
- S. Little, D. Walter, C. Myers, and T. Yoneda, "Verification of analog and mixed-signal circuits using timed hybrid Petri nets," in *Second International Symposium on Automated Technology for Verification and Analysis (ATVA)*, 2004, pp. 426–440.

## Honors, Awards, and Achievements

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- Member & Chairperson of the C.S. Undergraduate Student Advisory Committee 1999–2001
- Presidential Scholarship at University of Utah 1996–2000
- College of Engineering HP/Whitaker Scholarship 1998–1999
- Clyde Christenson College of Engineering Scholarship 1995–1996