

David C. Walter

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Education

Ph.D. Computer Science (August 2007)
University of Utah, Salt Lake City, Utah

B.S. Computer Science (May 2001)
University of Utah, Salt Lake City, Utah

B.S. Computer Engineering (May 2001)
University of Utah, Salt Lake City, Utah

Dissertation

Dissertation Title: Verification of Analog and Mixed Signal circuits using Symbolic Methods
Dissertation Advisor: Professor Chris J. Myers

With the rapidly increasing complexity of hardware, traditional validation techniques are becoming insufficient. This has led to a substantial interest in the formal verification of digital components. There has been relatively little research, however, into the application of formal verification methods to the analog/mixed-signal domain. Therefore, the overall goal of this work is to provide a system for efficient and meaningful analysis of analog/mixed-signal circuits. This encompasses two major efforts: modeling and symbolic analysis.

The continuous nature of analog circuits requires a modeling method that is capable of representing continuous behavior and the discrete nature of digital circuits requires a modeling method that is capable of representing discrete behavior. This dual requirement necessitates a hybrid model—a model that can simultaneously represent continuous and discrete behavior. This work details the development of a specialized hybrid Petri net model with capabilities similar to hybrid automata.

Analysis is greatly complicated by the addition of continuous behavior to the model. To help alleviate this, infinite numbers of states are often grouped into equivalence classes represented by symbolic structures. The analysis methods described here represent ranges of continuous variables using groups of inequalities which are then either mapped to Binary Decision Diagram variables so that necessary operations can be performed efficiently, or handed over to an advanced Satisfiability Modulo Theories solver for analysis.

After describing the verification system in detail, experiences applying the techniques to several case studies are described and performance results are provided.

Awards

Presidential Scholarship, *University of Utah* (1996–2000)
College of Engineering HP/Whitaker Scholarship, *University of Utah* (1998–1999)
College of Engineering Clyde Christenson Scholarship, *University of Utah* (1996–1997)

Academic Service

Reviewer, *IEEE Transactions on Software Engineering* (2004)
Chairperson, CS Undergraduate Student Advisory Committee, *University of Utah* (2000–2001)
Member, CS Undergraduate Student Advisory Committee, *University of Utah* (1999–2000)

Professional Affiliations

Student Member, ACM (2005–2007)
Student Member, IEEE (2005–2007)

Research Experience

Research Assistant, Professor Chris Myers, *University of Utah* (January 2003–May 2007)

- Developed hybrid Petri net (HPN) model for modeling analog and mixed-signal circuits.
- Developed symbolic model-checking tool based on BDDs for analyzing HPNs and hybrid automata.
- Applied abstraction techniques to improve analysis performance and analyze large models.
- Applied these techniques to several hybrid systems and analog/mixed-signal circuits.

Teaching Experience

Instructor, Introduction to C++, *University of Utah* (Summer 2002)

- Course consisted of 40-50 primarily non-computer science majors.
- Lectured twice weekly and prepared weekly labs in cooperation with teaching assistant.
- Wrote homework assignments and exams, and developed course grading criteria.
- Content included C++ syntax, control structures, recursion, and dynamic memory allocation.

Instructor, Introduction to Java, *University of Utah* (Summer 2001)

- Course consisted of approximately 30 primarily non-computer science majors.
- Developed and presented all course content.
- Taught Java syntax; use of conditionals, loops, and methods; and object oriented design principles.

Teaching Assistant, *University of Utah* (September 1997–December 2002)

- Computer Engineering Senior Project, Bruce Boyes (Fall 2002)
- Computer Science Senior Project, Dr. Ellen Riloff (Spring 2002)
- Software Practice, Dr. Art Lee (Fall 2001)
- Digital System Design, Dr. Erik Brunvand (Spring 2000)
- Introduction to Computer Science I, Dr. Dave Hanscom (Fall 1999 and Autumn 1997)
- Introduction to Computer Science II, Dr. Dave Hanscom (Spring 1999 and Winter 1998)
- Lead labs of 10-30 people on topics including software engineering to digital logic design.
- Provided one-on-one assistance to students with questions.
- Graded exams and homework assignments.

Professional Experience

Student Consultant, *Microsoft*, Salt Lake City, Utah (August 2000–May 2001)

- Assisted faculty in integrating Microsoft technology into appropriate curriculum.
- Presented technical talks on the C# programming language.
- Organized events to promote student interest in Microsoft technology.

Software Design Engineer in Test (Intern), *Microsoft*, Seattle, WA (May 2000–August 2000)

- Worked in Windows CE Tools group to develop test plan for new project.
- Investigated testing methodologies of similar projects for possible use.
- Central contact person in testing team for project's management and development teams.

Software Design Engineer in Test (Intern), *Microsoft*, Seattle, WA (May 1999–August 1999)

- Worked in Windows NT Build group helping to streamline nightly build process.
- Developed web application to manage source code check-in process.
- Gained experience using Active Server Page and SQL Server technology.

Technical Writing Co-Op, *Unisys*, Salt Lake City, Utah (June 1997–September 1997)

- Wrote and edited technical documentation for products ranging from peripherals to mainframes.

Publications

Journal Articles

- C. Myers, R. Harrison, D. Walter, N. Seegmiller, and S. Little, “The case for analog circuit verification,” in *Electronic Notes in Theoretical Computer Science* (ENTCS), June, 2006, 153(3): 53–63.
- H. Zheng, C. Myers, D. Walter, S. Little, and T. Yoneda, “Verification of timed circuits with failure directed abstractions,” in *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* (TCAD), March, 2006, 25(3): 403–412.

Conference Papers

- D. Walter, S. Little, N. Seegmiller, C. Myers, and T. Yoneda, “Symbolic model checking of analog/mixed-signal circuits,” to appear in *12th Asia and South Pacific Design Automation Conference* (ASPDAC), January, 2007, pp. 316–323.
- S. Little, N. Seegmiller, D. Walter, C. Myers, and T. Yoneda, “Verification of analog/mixed-signal circuits using labeled hybrid Petri nets,” to appear in *International Conference on Computer-Aided Design* (ICCAD), November, 2006, pp. 275–282.
- S. Little, D. Walter, C. Myers, and T. Yoneda, “Verification of analog and mixed-signal circuits using timed hybrid Petri nets,” in *Second International Symposium on Automated Technology for Verification and Analysis* (ATVA), 2004, pp. 426–440.
- H. Zheng, C. Myers, D. Walter, S. Little, and T. Yoneda, “Verification of timed circuits with failure directed abstractions,” in *IEEE International Conference on Computer Design* (ICCD), 2003, pp. 28–35.

Workshops

- D. Walter, S. Little, N. Seegmiller, and C. Myers, “Symbolic model checking of hybrid Petri nets using BDDs,” at *SRC Student Symposium*, October, 2006.
- C. Myers, R. Harrison, D. Walter, N. Seegmiller, and S. Little, “The case for analog circuit verification,” in *The Workshop on Formal Verification of Analog Circuits* (FAC), April, 2005.
- D. Walter, S. Little, N. Seegmiller, and C. Myers, “Symbolic model checking of hybrid Petri nets using BDDs,” at *TECHCON 2005*, October, 2005.